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TNG New Generation CCD Controller

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Abstract: The CCD manufacturers have improved the scientific CCD in terms of number of pixels, readout speed and noise. 4K×4K 2 outputs CCDs are currently available and show a readout noise less than 5 electrons r.m.s. at a readout speed of 1 Mpixel/s.

To take full advantage of the CCD technology improvements an "up to date" CCD controller will be needed. Thus, at the TNG, we decide to design a new CCD controller able to drive quickly large area CCDs as well as mosaics without degrading the readout noise allowed by these new CCDs. In this paper we describe briefly the design through a schematic diagram and the expected performances.

1. INTRODUCTION

At the Telescopio Nazionale Galileo (TNG), the Italian national facility located at Roque de los Muchachos in La Palma (Canary Islands, Spain) three scientific instruments, having CCDs as detectors, finally will operate for photometric and spectrographic observations. One of those that currently is working, is the optical imager (OIG) that has a mosaic of two 2K×4K EEV 4280 CCDs, the other two that will be in operation on summer next

year, are the low resolution spectrograph (LRS) equipped with a 2K×2K LORAL CCD, and the high resolution spectrograph (SARG) equipped with a mosaic of two 2K×4K EEV 4280 CCDs.

Actually to read the two EEV chips of the OIG, our CCD controller developed many years ago (details in Bonanno et al. 1995 and in Bortoletto et al. 1996) allows to read the whole image in about 250 seconds. This time, of course, is not adequate with the current readout allowed by new CCDs.

To take full advantage of the CCD technology improvements a new CCD controller able to drive quickly large area CCDs as well as mosaics without degrading the readout noise has been designed. The compactness, the weight, the speed and the noise performance are driven the design. The idea is to provide all digital sequences for the CCDs, from an interface located on the host computer, and connect the CCD electronics through an high speed full duplex fiber link.

With a Correlated Double Sampler (CDS) of 2.5 μs at minimum, this new CCD controller will allow an acquisition rate 400 Kpixels/s per channel, and thanks to the high speed link, many and many channels will be read at a time, very useful for large mosaics.

2. THE CCD CONTROLLER

As stated above the design of the CCD controller is driven by the idea to have all digital signals as well as the sequences generator, a Digital Signal Processor (DSP), on board of the host computer interface. The signals will be replicated on the SEQUENCER board that provides also the clocks to the CCD, in fact the board has digital-to-analogue converters for the upper and lower level voltages of the clocks.

We adopted the PCI bus standard to interface the CCD controller to the host computer. The AMCC S5933 PCI matchmaker controller chip is used for this purpose.

To handle the incoming data we use a FIFO memory and the AMCC S5933 chip. The data rate on the bus is 33 MWords/sec (Word of 32bits) and a Win 9X, Win NT driver has been developed to store the data pixel on the PC memory.

The CCD controller, excluding the power supply, is constituted essentially by three electronic boards: two double euro-card and one extended PCI board, figure 1 shows a schematic diagram of all the architecture.

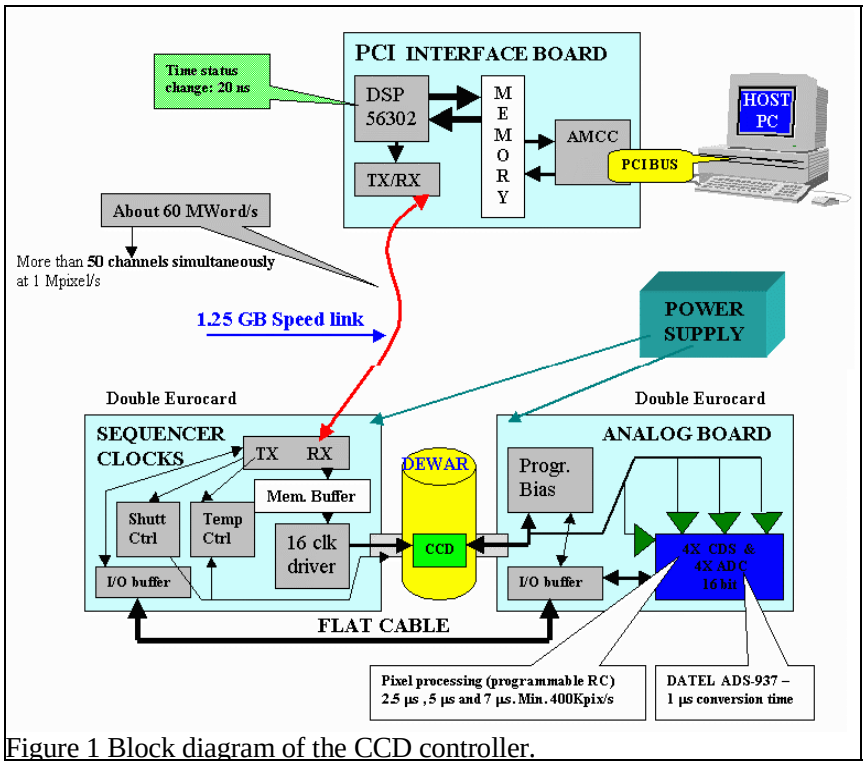

Figure 1 Block diagram of the CCD controller.

The three board are:

1. A PCI board based on the DSP Motorola 56302 that provides all digital sequences to drive CCDs. An AMCC S5933 PCI controller is used to interface a PCI bus. A transmitter/receiver chip set based on the HDMP 1022 (21 bits data parallel-to-serial) and on the HDMP1024 (21 bits serial-to-parallel) manufactured by HP and a fiber optic provide a fast link with the two other boards.
2. A CCD Sequencer Board/Clock driver that receives all sequences from the PCI board and replicate the signals delivered by the DSP. This board provides also all needed signals to generate 16 clocks.
3. An Analog Board that provides 8 programmable bias and allow to process and acquire four different video channels. The Corelated Double Sampling (CDS) technique has been adopted, and a time constant can be programmed from 7 to 2.5 µs. Furthermore each analog board is able to host four 16 bits Datel ADS 937 ADCs (conversion time of 1 µs), and 8 anolog board can be controlled simultaneously.

This architecture allows to drive a mosaic of four CCDs with one output or a mosaic of two CCDs with two outputs. by using just two boxes connected directly at the CCD dewar. Only two fibers will link the CCD controller to the host computer, one to send the digital sequences and one to receive the data pixel. A flat cable connect the analog box to the sequencer box to send the acquired and converted pixel signal.

3. EXPECTED PERFORMANCES

From a mechanical point of view the system will be very compact in fact just two box will be connected directly to the dewar and no other cabling except a fiber and few wires for power supply are required.

From an electronic point of view the system becomes less noise sensitive because all analogue electronics is close the CCD. And thanks to this unique architecture we are encouraged to use switching power supply instead of that linear. We are confident that this architecture has an intrinsic noise immunity and will be able to guarantee the noise figure showed by current available CCDs.

As said on the previous section, the sequencer can address 8 analog boards simultaneously and thus a maximum of 32 channels can be acquired once at a time. This means that with a sequencer and 8 analog boards it is possible to drive 16 CCDs with two outputs. To acquire other 32 channels another sequencer will be required. The high speed link is capable to sustain 64 channels at a 400 Kpixels/s, and as can be easily computed the PCI board can handle all the channels.