A new Photon Counting Detector: Intensified CMOS-APS

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Abstract: A new type of position sensor (Complementary Metal Oxide Semiconductor Active Pixel Sensor or CMOS-APS) used as readout system in MCP-based intensified photon counters, is presented in this paper. Thanks to the CMOS technology, the pixel addressing and the readout circuits as well as the analogue-to-digital converters are integrated into the chip. This unique characteristic made the CMOS-APS a good candidate to make a very compact, low power consumption, photon counting system. The main differences respect to the more classical Photon Counting Intensified CCDs (PC-ICCD), the selected CMOS-APS, the driving and interface electronics based on FPGA, the adopted algorithm to compute the center of the luminous spot on the MCP phosphor screen, are described.

Key words: CMOS-APS, Intensified Photon Counter

1. INTRODUCTION

In a photon counting system, several advantages of using a CMOS-APS instead of a CCD can be pointed out. In the CCD the charge is shifted sequentially from a pixel to the successive until it reaches a single (or a small number of) output node, while in the APS the charge in each pixel can be readout by addressing directly the pixel, being the preamplifier integrated on each pixel and the timing control and pixel addressing integrated on chip. Thanks to the CMOS technology, the pixel processing and the analogue-to-digital converters are integrated into the chip. The highly parallel structure of the APS allows a count rate dynamic range larger than that obtainable with photon counter based on intensified CCD. Other two important

characteristics, that are fundamental in space applications, have to be added: CMOS devices use a single 3.3 V power supply and show a better radiation hardness than CCDs.

The CCD technology, developed more than twenty years ago and improved during these years, is well known and is appreciated in many fields for the high quantum efficiency and the low readout noise even at relatively high scan rates. The novel CMOS-APS technology is in continuous evolution (see J. Janesick this volume), and, at the moment, a slight higher readout noise characterizes this technology. But this parameter, in photon counting systems can be overcome by setting a higher MCP gain. The other difference, in favor of CCD, is the fill factor that while for the CCD is 100 %, for the CMOS-APS is not higher than 60 %. However this parameter is not very critical for the performance of intensified systems.

2. THE CMOS-APS PHOTON COUNTING SYSTEM

The developed system is basically constituted by a Micro Channel Plate (MCP) with a phosphor screen coupled to a CMOS-APS through a relay optics. A block diagram of the complete system is shown in figure 1.

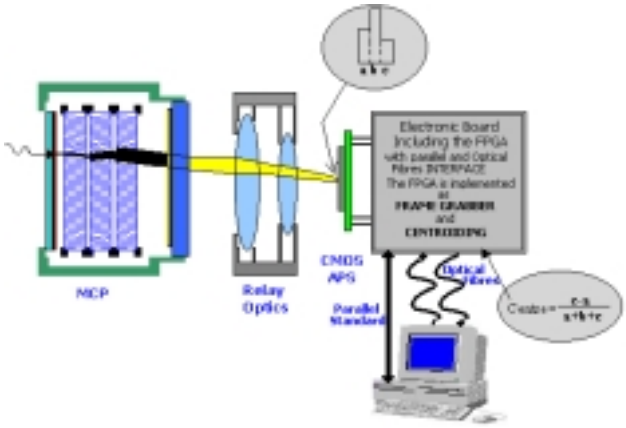

Figure 1 - Block Diagram of the CMOS-APS photon counting system

The electrons generated in a photocathode are multiplied by the MCP, and the emerging electron cloud impinges on a phosphor screen giving a luminous spot. A relay optics re-images this spot onto the CMOS-APS. The APS and a high density Field Programmable Gate Array (FPGA) are located on the same board that is connected to a PC through a parallel interface and a fast serial connection (1.2 GBit/s) based on fiber optic. The FPGA is configured to drive the APS, readout the pixels and make computations. The various functions are obtained by downloading

the configuration file via the parallel interface by using a standard protocol or via the optical fibers by using a dedicated DLL. Finally the data corresponding to the coordinates of each valid event are acquired by the computer and stored in a file.

2.1 Optical and mechanical layout

The CMOS-APS is delivered covered with a window, and, as for the CCDs, we planned to replace the window with a fiber optic taper. For the first operations we decided to use a well designed optical objective the Rodenstock model HR-Heligaron 35 with a very small numerical aperture better spatial resolution) and few optical components (minimizing the signal loss due to the transmittance of each element). The main characteristics of this objective are shown in table 1. Figure 2 shows the mechanical layout.

First lens diameter	31 [mm]
Max object diameter	35 [mm]
Field image diameter	8 [mm]
Total number of lenses	9
Transmission @ 550 nm	>98 [%]
Focal length	17 [mm]
Numerical Aperture	0.32
Demagnification	1 : 4.3
MTF @ 33.5 lp/mm	90 - 85 [%]
MTF @ 67 lp/mm	80 - 50 [%]
Relative Brightness	99.5 [%]

Table 1 – Characteristics of the HR-35

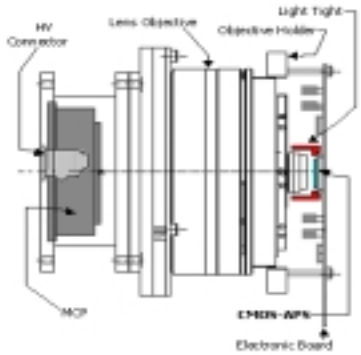

Figure 2 – Mechanical layout of the system

2.2 The CMOS-APS

As position sensor of the photon counting system we used the CMOS-APS PB-1024 manufactured by Photobit that with 500 frames/s assures a high count rate and thus increases the system dynamic range. The internal architecture is shown in figure 3. The PB-1024 has been designed to have a pixel row parallelism, in fact it includes on chip the timing and control circuitry to treat a row at a time (see the Row Timing Block on the schematic), and 1024 8 bit-A/D converters are implemented to digitize simultaneously the analog signal from an entire pixel row. Furthermore the chip contains special self-calibrating circuitry that allows to reduce the fixed pattern noise. To speed-up the data output a “ping pong” memory array is used. This last stores the 1024 8-bit digitized data and is read during a next conversion cycle. Height pixel (a 64 bit word wide) at a time can be read through the eight ports of 8 bits. Thus in 128 clock pulses an entire row is read-out

The device can be considered as a “digital device” in the sense that it receives digital signals and send digitized data. Thus, to drive the sensor only a “digital controller” is required, as for example a Field Programmable Logic Array (FPGA).

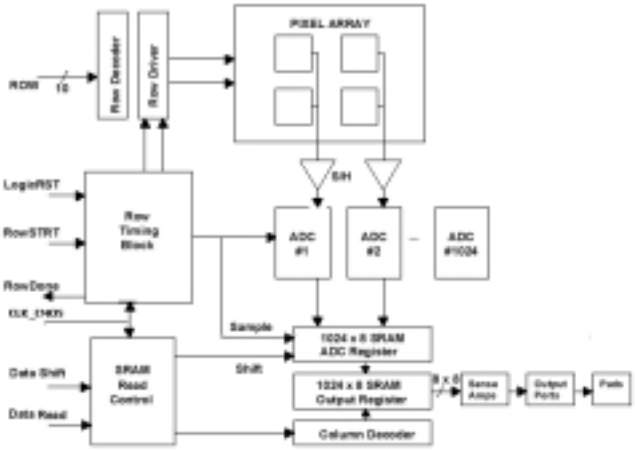

Figure 3 – Block diagram of the internal architecture of CMOS-APS PB-1024

3. THE CMOS-APS DRIVING ELECTRONICS

The block diagram of the entire board that constitutes all the detector front-end electronics is shown in the left panel of the Figure 4, while the right panel shows a picture of the developed board.

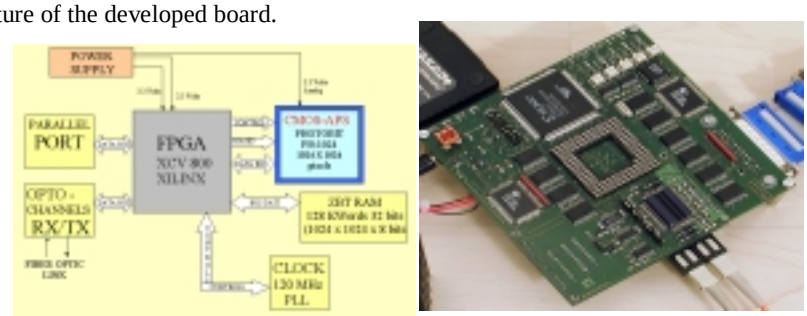

Figure 4 – Block diagram (left panel) and picture of the electronic (right panel).

The APS has on chip almost all the electronics needed to operate as an imager, the FPGA provides the rest of necessary signals. Furthermore the FPGA provides for the bias signals and the telemetry of the same signals together with those of the power supply. The circuits that realize the host PC interface via a standard parallel and a fast fiber optic link are also implemented on the FPGA. A 128 KWords 32 bits ZBT RAM is used to store the acquired image to be subsequently read at a different data rate. The heart of the controller is constituted by the implementation on the FPGA of the centroid algorithm. Essentially the centroid algorithm is divided into

two parts: the event validation that consists in locating the peak signal of all events above a specific discrimination level, and the centroid computation that is a three point truncated center of gravity that means if a, b, c, are the values with b being the highest, the center will be **(c-a)/(a+b+c)**. Figure 5 shows the block diagram of the FPGA circuit implementation.

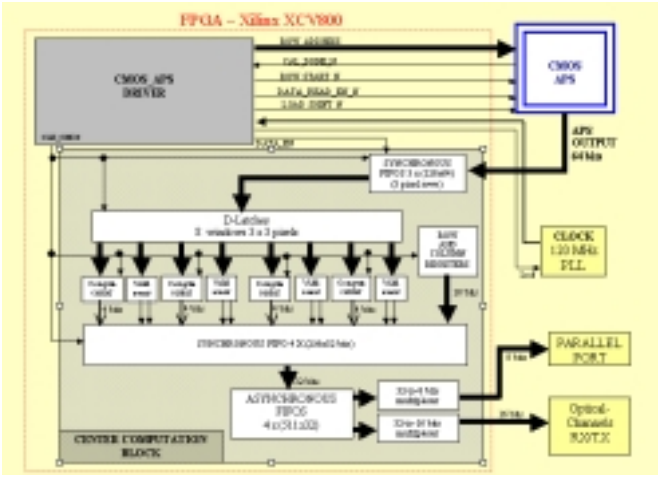

Figure 5 – Block diagram of the FPGA circuit implementation for the centroiding.

The 64 bits data, corresponding to 8 pixels, are stored on synchronous FIFOs at each pulse of the *CLK_CMOS*, and when the first three rows are completely packed on FIFOs, the computation procedure goes on. A set of D-Latches are used to obtain 8 windows of 3X3 pixels. The center computation and the event validation circuits operate simultaneously on these 8 windows, and, at each clock pulse, other eight 3x3 pixel windows are stored in the D-Latches, and the process will continue until the end of frame. When the four synchronous FIFOs receive the validation event signal, they store the row and column data (contained in the respective registers) and the sub-pixel value (given by the center computation circuitry) to form a 32-bit word with the event x-y coordinates to be sent, through 4 asynchronous FIFOs and a multiplexer, to the host computer via the parallel interface or the fast serial link.

4. FIRST RESULTS

Before operating in centroid mode, we took lots of images in *Frame Grabber* mode, varying the MCP gain, the objective focus and the APS working frequency. From the analysis of the spot profile with respect to the noise level we derived the best operating conditions. An image of 512X512 pixel acquired at a frequency of 20 MHz is shown in the lower left panel of the Figure 6. Surface plots of sub areas of 150 X 150 pixels of images taken at 20 MHz, 40 MHz and 50 MHz are also shown.

The noise increases with the increasing frequency, while the events are always well discriminated.

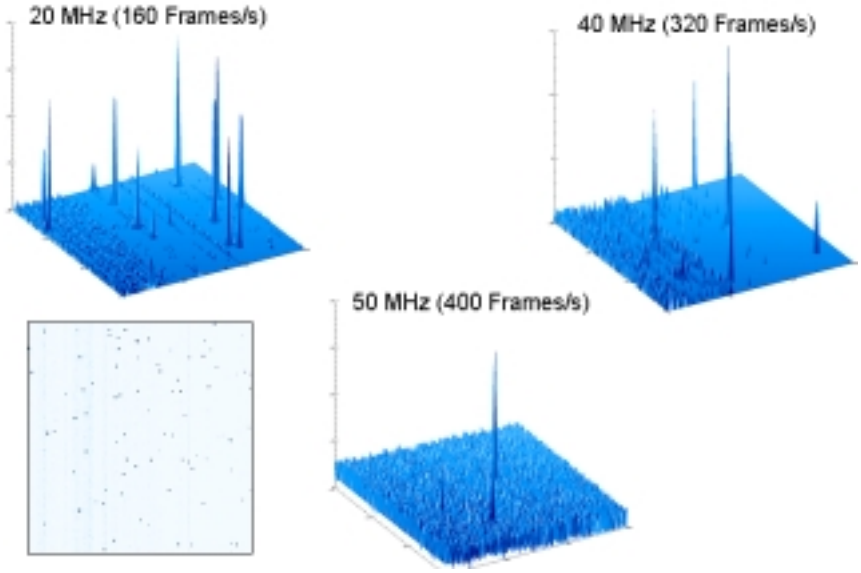

Figure 6 – Image of 512X512 pixel acquired at a frequency of 20 MHz and surface plots of sub areas of 150 X 150 pixels of images taken at 20 MHz, 40 MHz and 50 MHz.

The measured APS fixed pattern noise is negligible (3 - 6 ADU r.m.s.) at the working frequencies of 20 MHz (160 Frames/s), 40 MHz (320 Frames/s), and 50 MHz (400 Frames/s). A maximum APS working frequency of 50 MHz (400 Frame/s) is achievable without affecting the total noise and then the lower discrimination level. By windowing to half frame the system works at 800 Frames/s and a higher dynamic range is obtainable. And thus we can conclude that the CMOS-APS used as position sensor in MCP based systems can perform better than a faster CCD and with some important advantages: compactness, simplicity, radiation hardness (good for space applications) and low power consumption.