The architecture of the PLATO Instrument Control Unit

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ABSTRACT

The "PLAnetary Transits and Oscillations of stars" (PLATO) is one of the three selected candidates for the next M-class mission in the framework of the European Space Agency Cosmic Vision 2015-2025, currently expected for launching by the end of 2018. PLATO aims to find and characterize exoplanetary systems by detecting planetary transits and carrying out asteroseismology of their parent stars. The Instrument Control Unit (ICU) is part of the on-board Data Processing System and it is devoted to process and compress digital data inputs from 18 processing units, collecting analog data from 34 FPAs hosting 4 CCDs each. ICU will be also in charge of managing telemetry and telecommands to and from the Service Module (SVM) and to collect the payload's housekeeping and science data. This paper will describe the ICU architecture and functionalities addressing the mission scientific requirements.

Keywords: Exoplanets, Planetary Transit, Asteroseismology, Instrument Control Unit, Data Handling, Signal Processing, LEON2, SpaceWire.

1. INTRODUCTION

PLATO is one of three M-class space science mission of ESA's Cosmic Vision program under evaluation as candidates for the launch slots foreseen for the 2018. PLATO is a planet finder that will also address questions on the existence, distribution, evolutionary state, and characteristics of exoplanets in the solar neighborhood. Answers to these questions are essential to understand how planetary systems, including our own, are formed and evolve, and also as a first and necessary step to understand whether life can exist elsewhere in the Universe, and locate potential sites for life. Since the discovery of the first exoplanet in 1995, this field has seen a remarkable development, with more than 570 exoplanets currently known (early August 2011). Most of these objects are giant planets in close-in orbits, but continuous progress in the precision of radial velocity observations is now enabling the detection of "Super-earths", with masses just a few times that of the Earth.

One of the major goals of exoplanet research is to identify the population of exoplanets in the solar neighborhood and beyond, and determine their physical characteristics, including their internal composition. This goal can only be reached if the basic planet parameters, namely their radii and masses, can be measured to a sufficient accuracy. Subsequently, the mean planet density will be determined well enough to constrain models on its internal structure and composition.

1.1 Basic science goals and objectives

The main goal of PLATO is to detect and characterize a large number of exoplanets through their transits in front of their host stars, and provide measurements of their radii and masses, hence of their mean densities [1].

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In order to make these measurements possible, PLATO will focus on bright stars, at least 3 to 4 magnitudes brighter than the targets of the previous missions, and it will also explore a target list including a large sample of very bright (mV ≤ 8) and nearby stars, as well as a large sample of very nearby M dwarfs.

The brightness of the PLATO targets will bring three key advantages:

1. the ground based follow-up observations will be highly facilitated, and the required precision will be reached to confirm small, terrestrial planets in the habitable zone and to measure their masses;

2. the host stars of the detected planets will be studied in detail, in particular via seismic analysis using the PLATO data themselves; seismic analysis, i.e. the measurement of stellar oscillations, will be used to probe the internal structure of these stars, and determine their radii, masses, and age in a precise and reliable way;

3. the detection of exoplanets orbiting very bright and nearby stars, as well as planets around very nearby M dwarfs, will provide the best targets for subsequent detailed follow-up observations, both from space (e.g. JWST) and from the ground (e.g. E-ELT), including in particular spectroscopy of their surfaces and atmospheres, in the search for biomarkers.

The photometric transits detected by PLATO will be used to derive the ratio Rp/Rs of the planet radius to that of its host star. Follow-up observations from the ground will be used to measure the mass ratio Mp/Ms. The planet radius and mass will then be determined, using the radius and mass of their host stars derived from seismic analysis. Seismic analysis of the planet host stars will also allow us to determine the ages of exoplanetary systems, and therefore to place exoplanets in an evolutionary context.

Other main objectives of the PLATO mission are listed below:

- ✓ detection and characterization of Earth Analog systems;
- search for exoplanets around the brightest stars of solar type at all orbital periods and with all physical sizes;
 search for exoplanets around nearby M-type dwarfs with all physical sizes and at all orbital periods, including at orbital distances such that these planets fall within the habitable zones of these very cool stars;
- search for and characterization of exoplanets with a wide variety of sizes, masses and orbits around bright stars; \checkmark
- ✓ full characterization of very bright stars, of all masses and ages, using seismic analysis.

In addition to the seismic analysis of planet host stars, which represents the highest priority goal of the mission, asteroseismology of the many other stars present in the field of view will be used to study stellar evolution. Observations of stars of all masses and ages, all across the HR diagram, will be obtained to this purpose.

1.2 PLATO observational strategy and science data products

The PLATO science objectives will be met using long uninterrupted high precision photometric monitoring of large samples of stars. The science observations will be divided in two phases:

• the Long-Duration Observation Phase: two successive fields will be monitored;

• the Step & stare Observation Phase: extends the sample of stars surveyed for short period planets and for stellar structure studies, as well as for revisiting targets of the first two fields in an optimized way, to confirm longer period exoplanets.

As baseline PLATO shall perform two long monitoring phases of 2 years each, followed by a 2-year step & stare phase with a mixture of 5, 4, 3, and 2-month runs. Under these hypothesis, the overall field coverage of the mission would be about half the whole sky.

In order to detect and characterize planetary photometric transits, as well as to detect and measure stellar oscillations, PLATO shall provide ultra-high precision, long duration, uninterrupted photometric time-series of a large number of bright stars, in the optical wavelength domain. The basic PLATO data products will be white-light curves in the visible domain, star centroids and "imagettes" (small images of 7x7 and 9x9 pixels centered on the target stars).

2. THE PLATO PAYLOAD ELECTRICAL ARCHITECTURE AND THE ICU ROLE

2.1 The PLATO payload concept

In order to meet all the mission requirements and address the science goals, the proposed instrument concept is based on a multi-telescope approach, involving a set of 32 "normal" cameras working at a cadence of 25s and monitoring stars fainter than mV = 8, plus 2 "fast" cameras working at a cadence of 2.5s, and observing stars in the magnitude range 4 to 8 [2]. All the cameras are based on a fully dioptric telescope including 6 lenses, protected against radiation effects by a front window; each camera has an 1100 deg² field, and a pupil diameter of 120 mm.

The 32 normal cameras are arranged in four groups of 8 cameras. All 8 cameras of each group have exactly the same field of view, and the lines of sight of the four groups are offset by a 9.2° angle from the +Z axis. This particular configuration allows surveying a total field of about 2250 square degrees per pointing, with various parts of the field monitored by 32, 24, 16 or 8 telescopes. This strategy optimizes both the number of targets observed at a given noise level and their brightness.

Each camera is equipped with its own CCD focal plane array, including 4 CCDs having 4510 x 4510 pixel frame format, working in full frame mode for the normal cameras, and in frame transfer mode for the fast cameras.

There is one DPU (Data Processing Unit) per 2 cameras performing the basic photometric tasks and delivering a set of light curves, centroid curves and imagettes to the central Instrument Control Unit, which stacks and compresses the data, then transmits them to the SVM for downlink. Data from all individual cameras are transmitted to the ground, where final instrumental corrections, such as jitter correction, are performed (see Fig. 1).

The DPUs of the fast cameras will also deliver a pointing error signal to the AOCS, at a cadence of 2.5s. Several photometry algorithms (plain aperture photometry, weighted mask photometry, Line Spread Function fitting) are planned to run on board, each star being allocated one of them, depending on its brightness and level of confusion.



Figure 1. Overview of the PLATO data processing system architecture and of the data flow rates.

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2.2 Digital electronics

Digital functions are implemented into several units: the CCD image processing is performed by either the normal DPUs (located in the MEUs – Main Electronics Units) or by the fast DPUs depending on the cameras (either normal or fast). Then all the data processed by the DPUs are transmitted to the Instrument Control Unit for additional treatments. Each MEU hosts also two SpaceWire routers to merge the data from the 4 N-DPUs. A SpaceWire router unit is also implemented in each ICU (Nominal + Redundant) to merge data from the 4 MEUs and the 2 Fast DPUs. In order to improve the SpaceWire network redundancy scheme, the SpaceWire router unit of the ICU-N and the SpaceWire router of the ICU-R can be switched on simultaneously by the active ICU Processor Unit, and then work in hot redundancy. For commandability and monitoring purposes, the 4 normal AEUs (Ancillary Electronics Units) and the F-AEU, are also connected to the SpaceWire network (see Fig. 2).

2.3 ICU digital data streams

Due to the large number of cameras the data flow architecture is hierarchical: each camera owns its front-end electronics (FEE) in charge of reading out the four CCDs of a FPA. Therefore, each FEE includes a phase sequencer, 8 analog processing and 14-bit digitization electronics as well as adjustable biases.

In addition, each N-FEE includes two high performance SpaceWire bidirectional serial interface 1- to transfer to the digital electronics the digitized CCD raw data 2- to receive from the digital electronics (ICU) low level commands (mainly to configure the analog electronics) and 3- to transfer digital housekeeping to the ICU via the MEU routers. Digital data are then pre-processed in the N-DPU sub-systems of the MEU before sending them to ICU.

In addition each F-FEE includes 8 SpaceWire bidirectional serial interfaces 1- to transfer to the digital electronics the digitized CCD raw data 2- to receive from the digital electronics (ICU) low level commands (mainly to configure the analog electronics) and 3- to transfer digital housekeeping to the ICU via the F-DPU. Digital data are then processed in the F-DPU.



Figure 2. PLATO Data Processing System (DPS) overview.

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After processing, the digital data are gathered by ICU which is in charge of generating telemetry packets to the SVM mass memory. Similarly, all sub-system housekeeping parameters are gathered by ICU which is also in charge of generating corresponding telemetry packets and possibly performing actions related to instrument FDIR (Fault Detection, Isolation and Recovery).

Bidirectional data transfer between DPU and ICU is achieved by mean of 4 (MEU) + 2 (F-DPU) SpaceWire links.

Configuration commands are received by the ICU from the SVM. Then according to the destination, the command is processed and routed either to MEU, F-DPU, N-AEU, or F-AEU (see Fig. 2). Finally the command is routed to FEE (through DPU) when applicable.

3. THE ICU DIGITAL SIGNAL PROCESSING ARCHITECTURE

The actual ICU electronics architecture, proposed for the Definition Phase, is an update of the design produced during the Assessment study and it includes several improvements concerning optimization of the HW resources and the redundancy philosophy. This architecture has been updated in order to reduce complexity, power consumption, mass and overall dimensions. So, it can presently rely on a very simplified block diagram compliant with all the scientific and technological payload requirements.

The proposed ICU HW architecture is a good trade off between these requirements and the development plan and Model Philosophy, considering the engineering developments, costs and schedule related to the HW and technology recurrence.

3.1 Redundancy philosophy

PLATO ICU Main and Redundant Units will basically work in cold redundancy. So, at a given time, only one unit will be switched on. In order to improve redundancy, reduce the overall mass and avoid possible problems related to the interface management, the 2 ICU chains (M+R) are implemented in the same box with the capability to cross-strap the main and redundant modules, owing to the use of a motherboard for physical routing.

The ICU is, in principle, a single-point-failure-free internally redounded unit; redundant functions are housed on separate PCBs; any combination of cold redundant functions is possible in order to guarantee a reliable digital data collection and proper operations.

3.2 Requirements

The ICU Application SW (ASW) will manage all the Payload's electronics operational modes, each having its own functional requirements. Some requirements, common to all modes, are listed below. In particular ICU shall:

- handle the communication with spacecraft;

- receive and process telecommands: the received commands will be validated prior to their execution;
- format and transmit cyclic and sporadic housekeeping telemetry packets;
- format and transmit the scientific payload telemetry packets;

- manage the SpaceWire network: ICU is a remote network manager (router configuration, router monitoring, router status reporting, etc);

- receive the onboard time (Central Time Reference) from the SVM, handle the time stamping of the data transmitted in TM and forward the CTR to the DPUs;

- receive a SpaceWire time code from the SVM and forward it to the DPUs;
- produce state and diagnosis information (cyclic status, progress event);
- schedule the DPU tasks (by the way of commands sent to the DPUs);
- manage the digital data flow;
- manage the SW mode transitions;
- manage the SW parameters;
- manage the maintenance of the ICU SW;
- manage the maintenance of the N-DPU SW;
- manage the Star Catalogue;
- compress data using a lossless compression algorithm. A compression factor of at least 2 is required;
- acquire and transmit to SVM its own voltage and current consumptions.

3.3 Observational mode digital data processing

During the observational mode the ICU digital signal processing capabilities shall perform several time-series actions in order to address all the observational requirements. In particular:

- every 2.5s the active ICU processes the data (flux, centroids and imagettes) sent by the F-DPUs. The imagettes are compressed before being transmitted to the SVM. The flux and the centroids are stacked: N measurements are stacked for each F-DPU;

- every 25s the active ICU processes the data (flux, centroids and imagettes) sent by the N-DPUs. The imagettes are compressed before being transmitted to the SVM. An outlier detection is performed on the flux and on the centroids by comparing the data corresponding to the same star as sent from N cameras (N=8 or N=16 or N=24 or N=32). The selection criterion is based on the computation of the median of the N measurements and on the variance computed at the 25s cycle. The selected measurements are stacked;

- every 50s the active ICU performs a detection of the outliers on the flux and on the centroids of the F-DPUs (criterion based on the computation of the median of the N stacked measurements and on the variance computed at the previous 50s cycle). The mean and the variance of the k ($k \le N$) valid flux and centroids are computed. The computed data are bufferised waiting for compression and transmission to the SVM;

- every 50s the active ICU also processes the stacked data corresponding to the N-DPU samples which are sent in TM at the cadence of 50s. The mean of the k (k \leq M) valid stacked measurements (flux and centroids) are computed and bufferised waiting for compression and transmission to the SVM;

- every 600s the active ICU processes the stacked data corresponding to the N-DPU samples which are sent in TM at the cadence of 600s. The mean and the variance of the k ($k \le L$) valid stacked flux and centroids are computed and bufferised waiting for compression and transmission to the SVM.

3.4 ICU overall HW architecture

In order to perform all the previous digital signal processing tasks, the ICU HW architecture hosts three main electronics boards working in cold redundancy and a motherboard. ICU implements a Processor board, a Memory and IO board hosting the routers unit and a Power Supply board. The CPU board also perform the so-called "Supervisor Function" in order to collect housekeeping data and handle TM/TC.

ICU design is based on a fault-tolerant and high-reliability hybrid SpW network that relies on a "chains and rings" topology so, in principle, its CPU core acts as a network manager.

In order to manage the required SpW links, improve the SpW network reliability and the overall cross-strapping capabilities ICU will implement three SpW routers in the MEM&IO board, as input from 12 SpW links (4 MEU + 2 F-DPU + 4 AEU + 2 F-AEU) and as output to SVM (TM links) and a router in the Processor Unit, as showed in the Fig. 3. Thanks to this configuration the overall ICU (M+R) can benefit from a fully cross-strapped architecture, so any electronic configuration is available in case of failure of one or more subsystems.

Every subsystem function hosts at least a Control and Configuration FPGA interfacing one or more SpW Routers in order to manage communications and perform primary tasks, like writing and reading SDRAM memory modules by means of their own parallel ports and FIFO interfaces, as illustrated in the following sections.

The main tasks performed by the ICU SpW network are:

- to access ICU internal Memory Unit by means of the write and read memory controller FPGAs and their parallel ports;
- to connect the Processing Unit 1 to the others Units;
- to connect the Processing Unit 2 (located in the redundant ICU) to the main network;
- to connect together the main and the redundant SpW multiplexing Units.

Two (M+R) independent SpW interfaces connect each ICU Processor board to the SVM On Board Computer (OBC) for TC reception and two (M+R) independent SpW interfaces connect each ICU MEM&IO board to the SVM Mass Memory for TM. Another SpW interface is provided for EGSE purposes. No SpW links between the ICU Processor Unit and the power Supply Unit have been included in the ICU design. They will be connected thanks to discrete line and/or serial interfaces.



Figure 3. PLATO ICU overall HW architecture.

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3.5 CPU board

The Processor Module shall implement an AT697F (LEON2) SPARC V8 micro-processor with RTEMS OS (as baseline). This Module is housed onto an extended double Eurocard PCB that is equipped with suitable connectors for internal connection to the Motherboard Unit and for I/O.

The ON/OFF switching of the Processor Module is achieved by switching on/off the associated DC/DC converter of the Power Supply module. The Processor Module with its own Monitoring Section and TM/TC capabilities perform the so-called Supervisor Function.

The processor includes on chip an Integer Unit (IU), a Floating Point Unit (FPU), a Memory Controller and a DMA Arbiter. Fault tolerance is supported using parity on internal/external buses and EDAC on the external data bus. Moreover the CPU itself provides:

- two 8-bits UART interfaces that can be used either for on-ground SW loading or for Debug with the SW Development & Maintenance facility;

- a Debug Support Unit;

- a J-TAG I/F, to interface the FPGA and the CPU.

The Processor Module also hosts the following memories:

- 128 KByte Boot PROM is provided for the bootstrap & initialization SW;

- 64 MByte NOR FLASH EEPROM is provided to store on board the ICU Application SW, the N-DPU ASW, the Star Catalogue and some configuration parameters. The NOR FLASH memory is randomly addressed and can be fully patched and dumped during flight by means of telecommands;

- at least 8 MByte SRAM is provided for ICU Application SW execution.

Both FLASH EEPROM and SRAM are protected by the processor EDAC which corrects any single bit error and alert on any double bit error detected. FLASH memories can be switched off when not accessed for long time in order to improve their data retention performance. The EEPROM On/Off switch is commanded through a GPIO line of the Processor.

3.6 Memory & IO board

The MEM&IO Module is arranged on an extended double Eurocard PCB. It is based on SDRAM memories that are assembled in 3D cubes.

The MEM&IO Module shall host (4+2) x 2Gbit Memory Cubes providing as baseline a usable memory capacity of 8Gbit. The I/F of such a Module are fully protected against failure propagation.

From the functional point of view the memory area is partitioned in sectors, being the sector the minimum area which can be allocated by the File Manager SW to a file/packet store. As baseline we consider a sector size of 1Mbyte.

The ICU proposed for PLATO hosts 2 fully independent MEM&IO Modules (1 operating and 1 cold backup) each providing a net usable memory capacity up to 8Gbit.

3.7 Power Supply board

The Power Supply module, which is implemented on an extended double Eurocard PCB, provides independent power supply to the two main functional blocks composing the unit:

- the Processor Module performing the Supervisor Function;

- the MEM&IO Module.

Therefore this module hosts two independent DC/DC Converters named SPV_DC/DC and MEM&IO_DC/DC. Redundancy is achieved by using two of these Power Supply modules. Each DC/DC converters can operate with a primary power bus in the range $23 \div 38V$.

Each DC/DC Converter can be individually switched ON/OFF: the SPV_DC/DC by means of external (from SVM) redundant Standard High Power ON/OFF commands while the MEM&IO_DC/DC by means of internal redundant low level commands generated by the Processor Modules.

Monitoring signals (that are secondary voltages, currents and temperatures) are provided to the Processor Module to be acquired (i.e. conditioned and A/D converted) by a Monitoring Section and C&C FPGA on the CPU board.

3.8 ICU SW architecture

There are four kinds of SW available to the ICU: the Bootstrap SW (BSW), the operating system (OS), the drivers and the Application SW (ASW). The BSW and the drivers will be provided by the ICU HW manufacturer; the OS depends on the adopted microprocessor but anyway will be a real-time OS commercially available, RTEMS as baseline. The drivers will be developed to be integrated in the OS.

The ASW code shall be written in C; some module maybe required to be written in Assembly.

The SW can also be seen as structured in layers; each layer offering services to the upward layer and exploits the devices of the downward one; this add a "vertical" modularity to the SW approach which fosters portability and maintenance.

The SW will be implemented following ECSS-E40 Part 1, as outlined in the Guide to applying the ESA software engineering standards to small software projects (BSSC(96)2, Issue 1. May 1996), ECSS-E-70-41A standards and PUS based applications.

The lowest level SW layer is the Board Support Package which maps the boards registers structure and supplies the routines needed to configure them. The HW Handlers layer holds the support code to perform basic operations on the HW, it also include the routines mapping the asynchronous interrupts generated by the modules.

RTEMS (Real-Time Executive for Multiprocessor Systems) is a real-time operating system designed for embedded systems. The directive execution times and other critical performance parameters such as interrupt latency are comparable to those of commercial executives. RTEMS offers very low overhead with useable configurations well under 32K and is deterministic with guaranteed execution times for nearly every operation.

The Basic SW, though separated, can also be considered as a part of ASW because it includes the services needed to fulfil the mission requirements, like: File Allocation Table management, memory patch and dump, memory scrubbing, SpW link management and so on.

The Application SW is the uppermost layer which interfaces the OBC and the DPS or camera chains. It implements the functions described by the high level mission requirements with a modular architecture.

3.9 Data compression

ICU shall perform a lossless data compression. This is a fundamental task of the ASW indispensable to reduce the overall amount of data before sending them to the platform central processing unit and from here to ground. In order to address the science, telecommands and housekeepings TM requirements at least a compression factor of two is required. This will be a fundamental task performed by the LEON2 CPU core running the ICU application SW. In order to support the SW compression task we are evaluating the possibility to implement aboard the CPU board a FPGA with DSP capabilities to compress and reduce the overall data amount following the best efficient way.

3.10 Budgets

The ICU power consumption will strongly depends on the overall maximum I/O throughput it has to sustain as well as on the used memory and CPU occupation rate. At present the ICU overall operational power budget is 19.8 W and is characterized by an overall mass of 6.5 Kg without contingencies.

These values are compliant with the Payload allocated power and mass budgets for ICU purposes as defined in the ICU Specification Document, following ESA constraints.

3.11 Mechanical design

As baseline the ICU Unit (M+R) is composed by 3 nominal + 3 redundant daughter-board modules perpendicularly plugged onto a motherboard that lays on the unit bottom (2 Power Supply modules, 2 Processor modules, 2 MEM&IO modules). The motherboard is fixed by screws to the unit bottom plate.

Each daughter-board is an extended double Eurocard module having motherboard connectors on one of the longest side and with the external I/O connectors on the opposite side (as baseline).

The daughter-boards are stiffened by a mechanical frame on which the external I/O connectors are fixed and screwed to the unit upper panels. The lateral sides of the modules support card-lock retainers that are used to fix the boards to the unit lateral panels.

All panels are made of aluminum alloy surface treated in according to MIL-C-5541 CL. 3 and then externally painted in black (except Bottom panel) to improve radiating exchange with the environment.

The panels thickness is designed to cope with the heat dissipation needs; in particular the thickness of the lateral panels increases from top to bottom to facilitate the heat sink.

4. CONCLUSIONS

Approaching the end of the Definition Phase, the digital signal processing architecture of the PLATO ICU is defined as reported in this paper as well in the "PLATO definition study report" (Red Book) [11]. From now to the Instrument Design Consolidation Review (IDCR), that will be held at the end of 2011, some minor HW modifications will be possible in order to fine address all the Mission scientific and technological requirements, waiting for the ESA working group/SSAC down selection of two of the three space missions to the next Implementation Phase.

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